QUEEN'S UNIVERSITY BELFAST

CWI CENTRE FOR WIRELESS INNOVATION

# COMPACT RF CMOS POWER COMBINERS WITH EMBEDDED HARMONIC TRAP

## Need

The demand for low-cost system-on-chips (SOC), which integrate digital, analog, and radio frequency (RF) circuitries on the same die, can only be met by CMOS processes due to their extremely small feature size. Smaller feature sizes are the focus of current research to meet the demand for faster circuitry and higher levels of integration, but this presents increasing challenges for RF designers. One major challenge in designing the RF transmitter of a CMOS SOC is that the output power of the power amplifier (PA) is constrained by the low transistor oxide breakdown voltages that limit the usable supply voltages. To prevent oxide damage and achieve the desired output power, multiple PA unit cells can be used together with power combiners, such as the Wilkinson power combiner (WPC), which inherently provides excellent impedance matching at both input and output ports, as well as high isolation between input ports, thus averting the load pulling between the PA unit cells. They are frequently used in various RF front-end transceiver circuits (e.g. power amplifiers, voltage-controlled oscillators, etc.), phased array radars, and other applications. They are however considered relatively large and too time-consuming to design, so there is a need to mitigate these problems.

## Approach

The CWI researchers have devised a thorough and concise methodology for correctly utilizing the mutual coupling of a coupled inductor in order to design compact lumped-element WPCs. Their analysis of mutual coupling showed that the parasitics of coupled coils could be exploited to provide the shunt isolation resistance, resulting in a "lumped-element WPC" requiring only three components, i.e. a coupled coil and two capacitors.

They also developed two distinctive circuit topologies, one employing a star inverting coupled coil (SICC), and the other employing a delta non-inverting coupled coil (DNICC), each with a variant containing a second harmonic trap to lower the total harmonic distortion (THD) and the required inductance value in the circuit. Hence, they designed in total four circuit prototypes operating in the 5 GHz frequency band, and fabricated them on TSMC's 28 nm bulk CMOS process.

The key design challenge was to achieve low insertion loss, high isolation, high return losses (low VSWR) at all ports, wide operating bandwidth, and reasonable levels of amplitude/phase balance, while keeping the overall circuit footprint minimal. The designs by CWI researchers have targeted 5-GHz WLAN (IEEE 802.11ac/n) applications, with the ultimate goal being to integrate the power combiners with high-efficiency switched-mode PAs, wherein isolation of at least 10 dB was needed to prevent one PA from loading the other.

## Results

1. Lumped-element WPC with world's smallest electrical area and added filtering functionality;
2. Systematic design methodology, simplifying optimisation process and reducing design time and time-to-market;
3. Compatible with most IC technologies, including low-cost high-integrated CMOS and III-V compound semiconductors such as GaN and GaAs.

## Demo video

n/a

## Publications

IEEE Transactions on Microwave Theory and Techniques (TMTT-2018-09-1107.R2), accepted 30 January 2019, (DOI: 10.1109/TMTT.2019.2903460)

Best Paper Award at the 25th IEEE International Conference on Electronics Circuits and Systems, December 2018

## Patents

1. UK Application No 1814756.1 (Sept. 2018)

## Researchers

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## Technology readiness level

1 2 3 **4** **5** 6 7 8 9